ISSN:0975-9646

Neha Goyal et al, / (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 5 (3) , 2014, 4200-4204

Study and Analysis of Universal Gates Using Stacking Low Power Technique

Neha Goyal[#1], Renu Singla[*2], Puneet Goyal[#3]

[#1, *2] *Department of Computer Science And Engineering, Shri Ram College Of Engg. & Mgmt, Palwal, India*

[#3]*Directorate General of Civil Aviation, New Delhi, India*

***Abstract*— The main objective of this paper is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level. Conventional NAND gate and Nor gate are designed snd then compared with the stack NAND and stack NOR using 180nm technology.**

Index Terms— **power, transistors, delay, CMOS, NAND Gate, NOR Gate, stacking, TANNER Tool, conventional.**

I. INTRODUCTION

Power consumption plays an important role in the present day VLSI technology[2]. Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost. If an IC is consuming more power, then a better cooling mechanism would be required to keep the circuit in normal conditions. Otherwise, its performance is degraded and on continuous use it may be permanently damaged[8].

II. OVERVIEW OF POWER DISSIPATION

It is more convenient to talk about power dissipation of digital circuits at this point. Although power depends greatly on the circuit style, it can be divided, in general, into static and dynamic power. The static power is generated due to the DC bias current, as is the case in transistor-transistor-logic (TTL), emitter-coupled logic (ECL), and N-type MOS (NMOS) logic families, or due to leakage currents. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. That is the reason why CMOS is the most suitable circuit style for very large scale integration (VLSI)[8].

CMOS is the logic family preferred in many designs due to following reasons:-

- Impeccable noise margins.
- Perfect logic levels.
- Negligible static power dissipation.
- Gives good performance in most cases.
- Easy to get a functional circuits.
- Lot of tools available to automate the design process.

III. STACKING TECHNIQUE FOR POWER REDUCTION

One technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [3].

Fig. 1 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in subthreshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach[3].

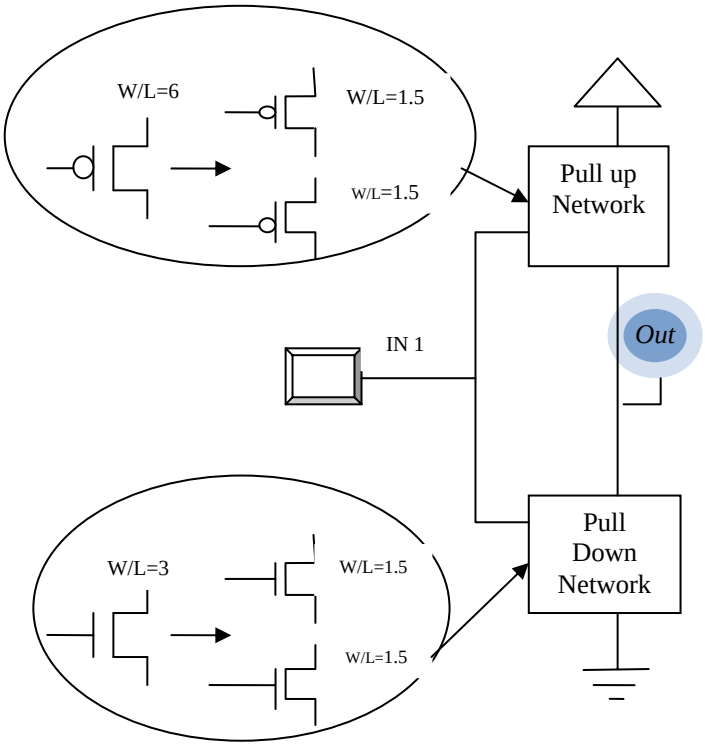

Fig. 1 A CMOS circuit using Stacking Approach

IV. PROPOSED WORK

Logic gates are fundamental building blocks of digital integrated circuits . Logic gate is idealized or physical device implementing a boolean function i.e, it performs a logical operation on one or more inputs and produces a single logical output. There are seven basic logic gates: NOT, AND, OR, NAND, NOR, XOR, XNOR.

In this paper we will be implementing Universal Gates gates: NAND, NOR.

A. NAND Gate

Operation When A=0 and B=0, both the nMOS transistors are OFF and both pMOS are ON. Hence, the output is connected to V_{DD} and we get logic high at the output .When A=1 and B=0, the upper nMOS is ON and lower nMOS is OFF, so the output cannot be connected to the ground. Under this condition left pMOS is OFF but right pMOS is ON. Hence, the output is connected to V_{DD} we get logic high at the output. When A=0 and B=1, the upper nMOS is OFF and lower nMOS is ON, so the output cannot be connected to the ground. Under this condition left pMOS is ON but right pMOS is OFF. Hence, the output is connected to V_{DD} we get logic high at the output. When A=1 and B=1, both the nMOS transistors are ON and both the pMOS transistors are OFF. Hence the output is connected to the ground and we get logic low at the output[3].

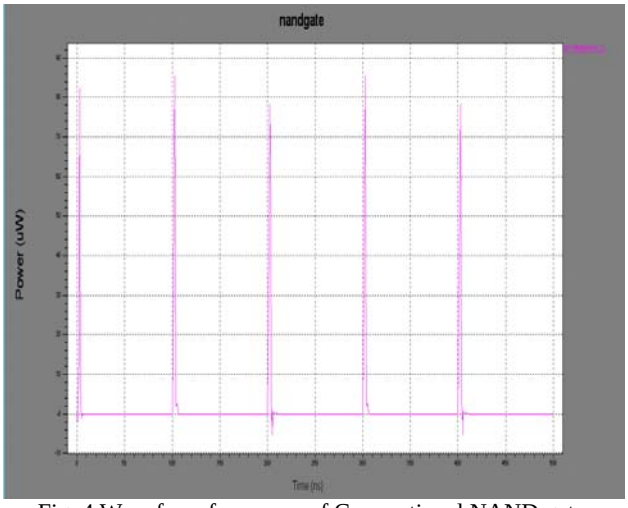

Fig .4 Waveform for power of Conventional NAND gate

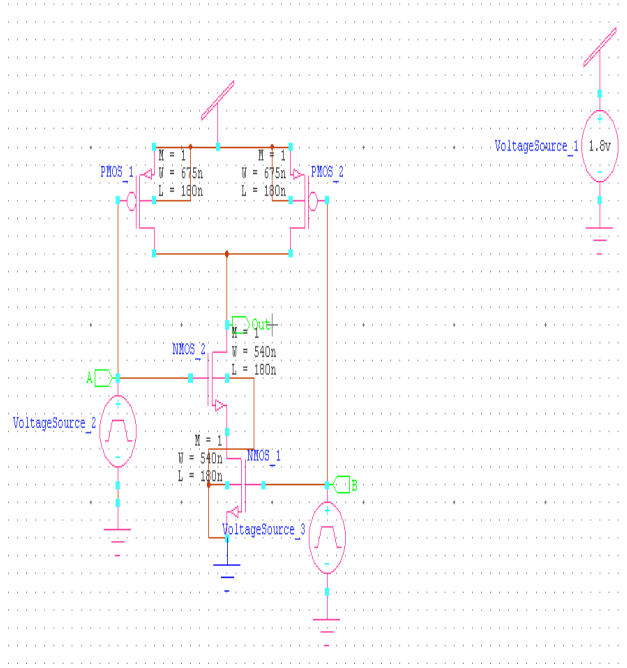

Fig. 2 Conventional CMOS NAND Gate

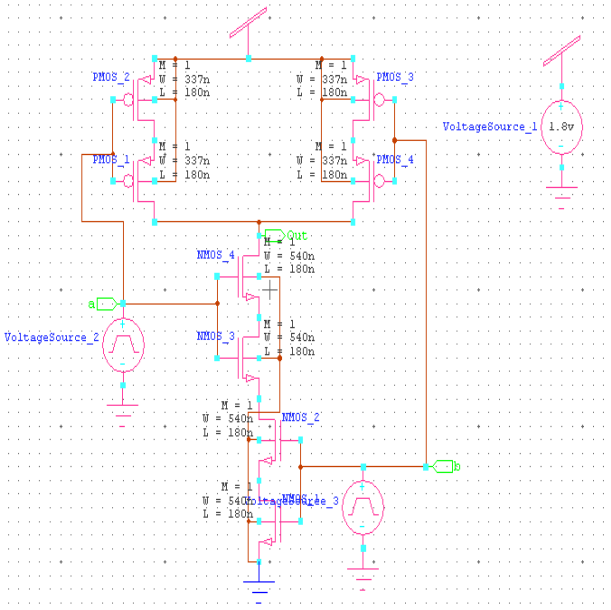

Fig. 5 Circuit for NAND gate using Stacking technique

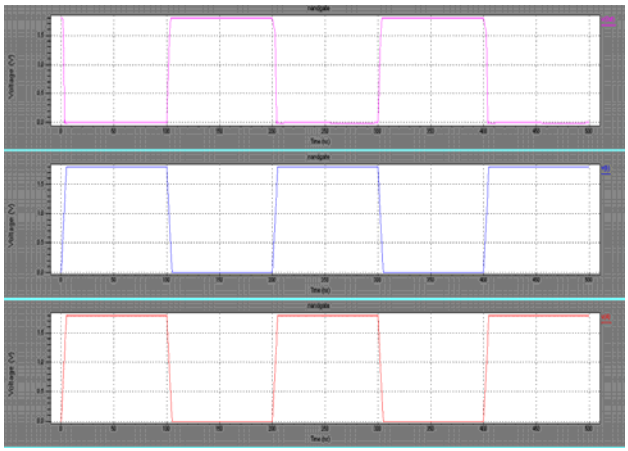

Fig. 3 Waveform for Voltage of Conventional NAND Gate

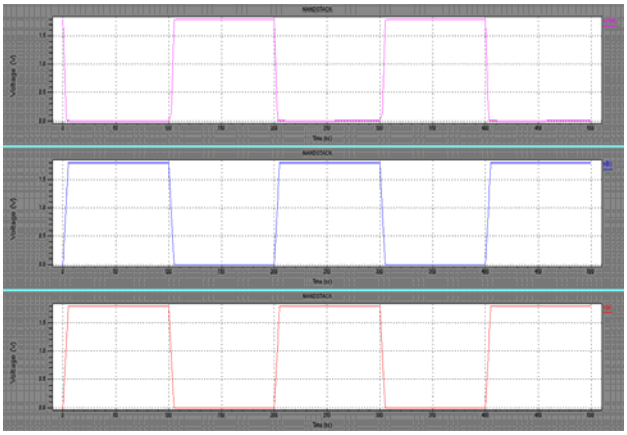

Fig. 6 Waveform for NAND gate Voltage using Stacking

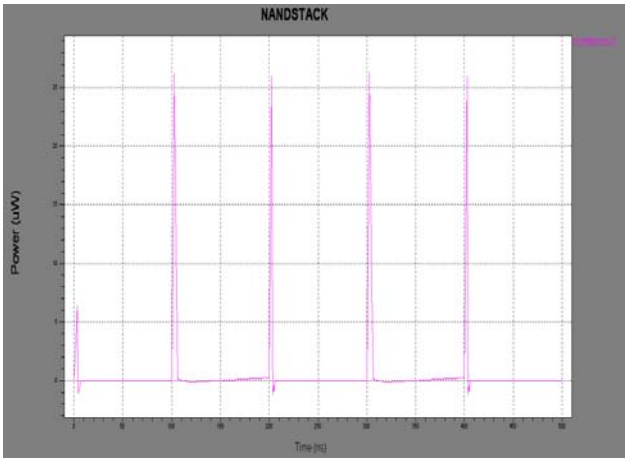

Fig. 7 Waveform for NAND gate Power using Stacking

B. *NOR Gate*

Operation: When A=0 and B=0, both the nMOS transistors are OFF and both pMOS transistors are ON. Hence, the output is connected to V_{DD} and we get logic high at the output.

When A=1 and B=0, the upper pMOS is ON and lower pMOS is OFF, so the output cannot be connected to the V_{DD} . Under this condition left nMOS is ON but right nMOS is OFF. Hence, the output is connected to ground we get logic low at the output.

When A=0 and B=1, the upper pMOS is ON and lower pMOS is OFF, so the output cannot be connected to the V_{DD}. Under this condition left nMOS is OFF but right nMOS is ON. Hence, the output is connected to ground we get logic low at the output.

When A=1 and B=1, both the nMOS transistors are ON and both the pMOS transistors are OFF. Hence the output is connected to the V_{DD} and we get logic low at the output[3].

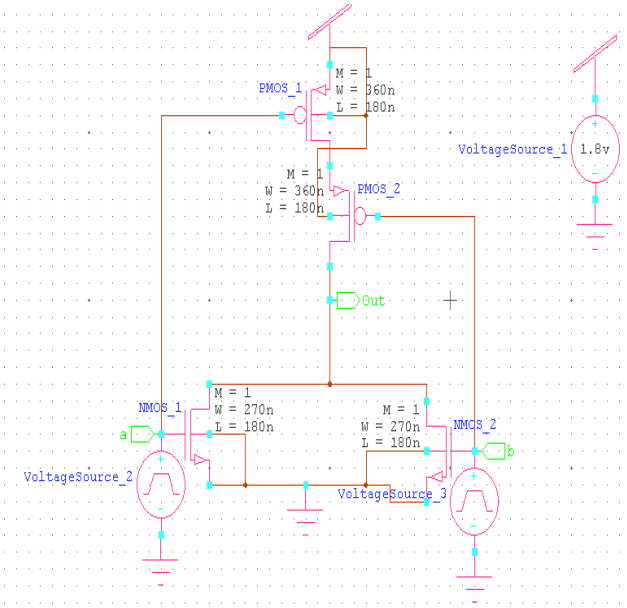

Fig. 8 A Conventional CMOS NOR Gate

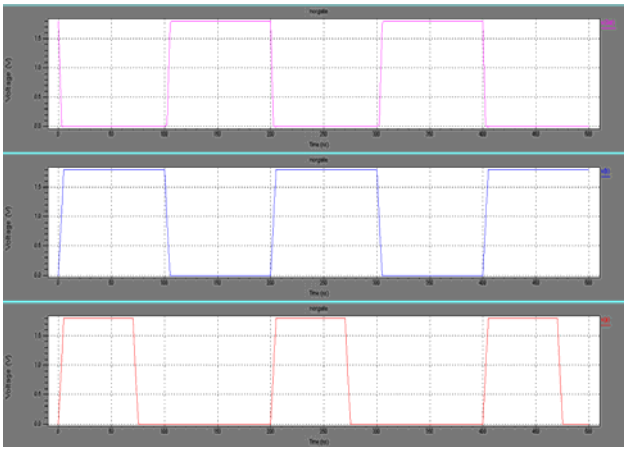

Fig. 9 Waveform for Conventional NOR gate Voltage

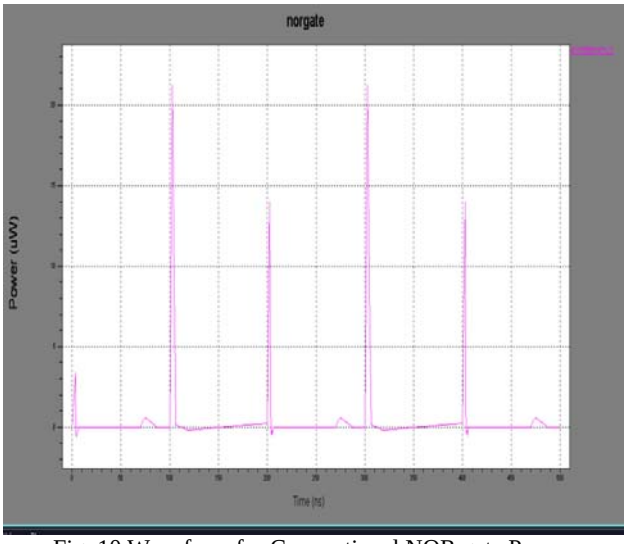

Fig. 10 Waveform for Conventional NOR gate Power

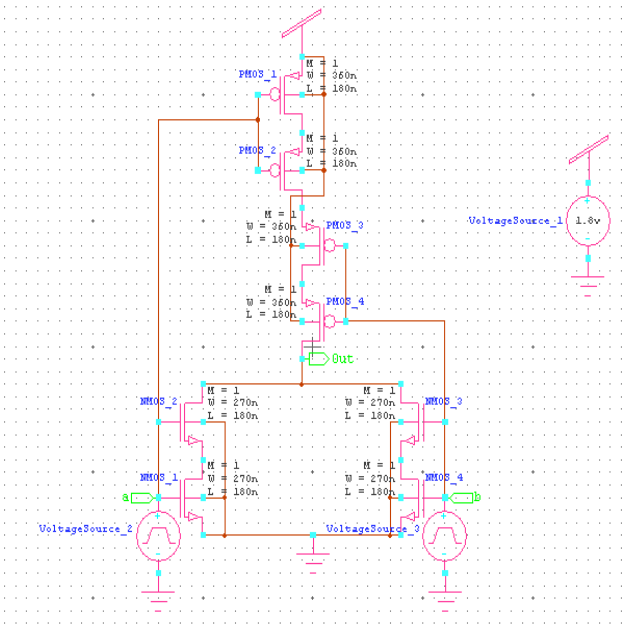

Fig. 11 Circuit for NOR gate using Stacking technique

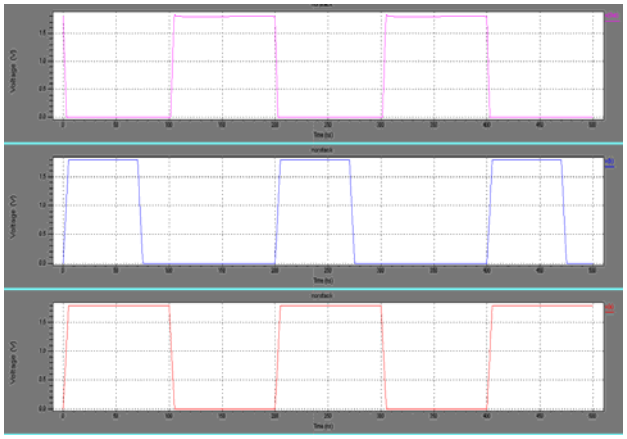

Fig. 12 Waveform for NOR gate Voltage using Stacking

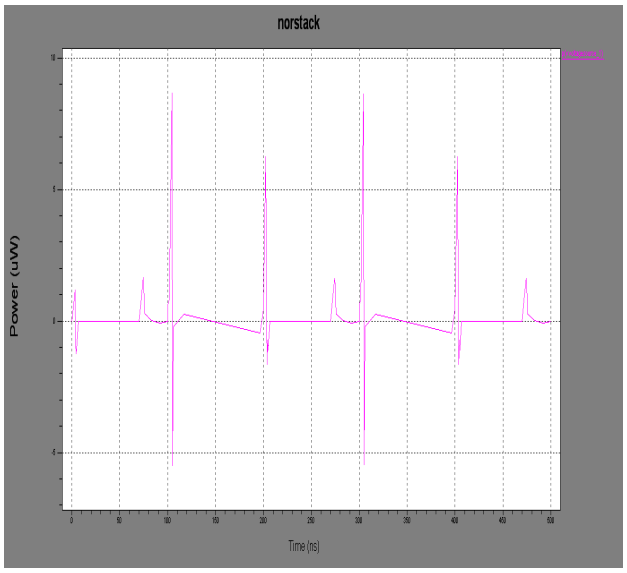

Fig. 13 Waveform for NOR gate power using Stacking

V. RESULTS

The Simulation of logic gates with and without low power techniques is carried out at 180nm, technology. CMOS technology parameters are taken for NMOS and PMOS transistors, using TSPICE tool. Transient Analysis is done to get Delay and Average Power results .

We have studied STACKING power reduction technique in this thesis and we compare this power reduction technique with CONVENTIONAL CMOS design.

TABLE I CMOS NAND GATE RESULTS

POWER REDUCTION TECHNIQUES	AVERAGE DELAY (In Nanoseconds)	AVERAGE POWER DISSIPATION (In Microwatts)
Conventional	0.36071	1.438965
Stacking	0.13260	0.5348692

TABLE II CMOS NOR GATE RESULTS

POWER REDUCTION TECHNIQUES	AVERAGE DELAY (In Nanoseconds)	AVERAGE POWER DISSIPATION (In Microwatts)
Conventional	0.17084	0.150228
Stacking	0.092349	0.1300761

VI. CONCLUSION

Comparison has been done for universal gates , delay and power is calculated for conventional and stacking circuits.

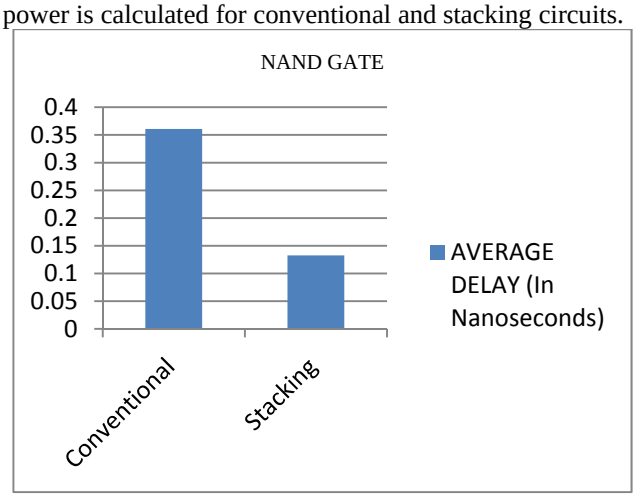

Fig. 14 Comparison of Average Delay for NAND Gate

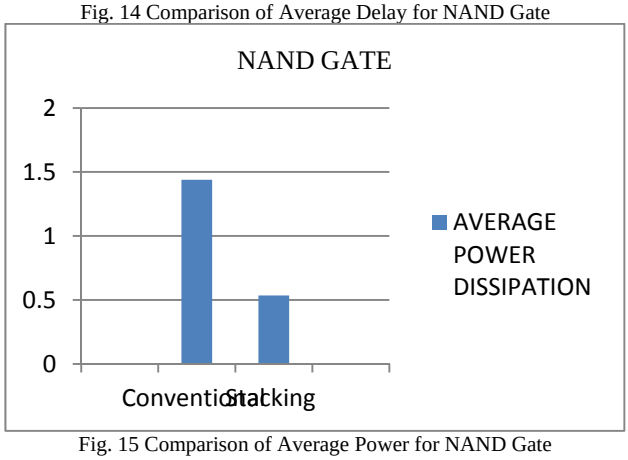

Fig. 15 Comparison of Average Power for NAND Gate

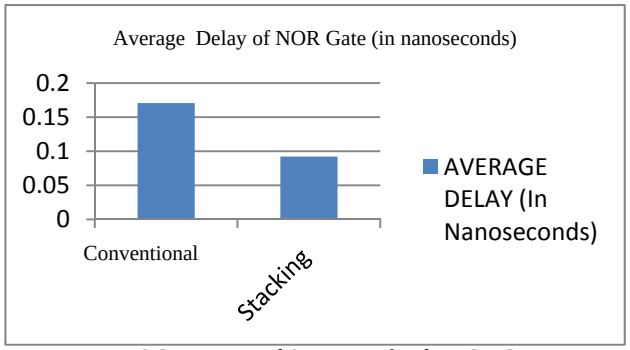

Fig. 16 Comparison of Average Delay for NOR Gate

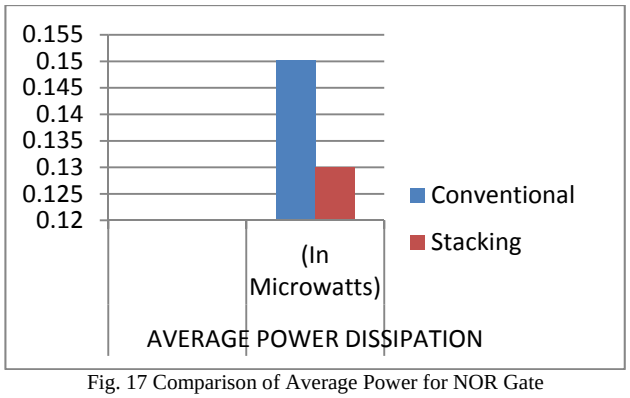

Fig. 17 Comparison of Average Power for NOR Gate

Implementing the STACK technique can reduce power dissipation of the LOGIC CIRCUITS. We can observe the reduction in power dissipation from Conventional to the Proposed Stack Technique in Logic Circuits. Delay can be minimized by increasing aspect ratio. The tool for simulation is TANNER and at 180 nm technology and the practical observations has been tabled.

REFERENCES

[1] B. Dilip, p. Surya prasad & r. S. G. Bhavani "Leakage power reduction in CMOS circuits using Leakage control transistor technique in nanoscale Technology" in International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, Vol-2 Iss-1, 2012.

[2] B.Yasoda1, S.Kaleem basha " Performance Analysis of Energy Efficient and Charge Recovery Adiabatic Techniques for Low Power Design" in IOSR Journal of Engineering (IOSRJEN) **e**-ISSN: 2250-3021, **p**-ISSN: 2278-8719 Vol. 3, Issue 6 (June. 2013), ||V1 || PP 14-21

[3] Debaprasad Das "VLSI Design" published by Oxford University Press 2010

[4] Harshvardhan Upadhyay, Abhishek Choubey, Kaushal Nigam "Comparison Among Different Cmos Inverter With Stack Keeper Approach In Vlsi Design"/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 3, May-Jun 2012.

[5] Jitender kumar1 , Dr.Munish Vashishath2, Nitin Sachdeva "Leakage Power Reduction in CMOS Logic Circuits by Transistor Stacking Technique"

[6] Krashna Nand Mishra"Efficient Carry Generation technique Incorporating Energy Recovering Logic Circuitry For Low Power VLSI." IEEE, 2008

[7] K.ROY AND S.C PARSAD "Low-Power CMOS VLSI Circuit Design", Wiley Publishers, New York, 2000

[8] Sandeep Kaushal "Comparative study and Analysis of Flip Flop Circuits for Power and Teamperature" M.Tech. thesis, YMCA Faridabad, India, May 2012 Sreenivasa Rao Ijjada,

[9] B.Ramparamesh, Dr. V.Malleswara Rao"Reduction of power dissipation in logic circuits" International Journal of Computer Applications (0975 – 8887) Volume 24– No.6, June 2011

[10] [Online].Available:http://docencia.ac.upc.edu/master/MIRI/NCD/assignments/Tema%201-EN.pdf.